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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Inventor: Anatoliy V. Tsyrganovich
	Group Art Unit: ~~2017~~ 2816
Frequency Locked Loop	Examiner name: ~~Unknown~~ HAI L. NGUYEN
	Attorney Docket No. ZIL-521-1P

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U.S. Patent Documents

*Examiner Initial		Number	Date	Applicants	Class	Subclass	Filing Date, If Appropriate
HLN	A	6,166,606	12/26/2000	Tsyrganovich	331	25	2/10/1999
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Foreign Patent Documents

		Document Number	Priority Date	Country	Applicant	Pub. Date	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

HLN	C	G. Fairhurst, "Phase Locked Loop (PLL)," United Kingdom, dated 1/10/2001, downloaded on 5/24/2004 from http://www.erg.abdn.ac.uk/users/gorry/course/phy-pages/dpll.html, 2 pages.
	D	T. Olsson and Peter Nilsson, "An all-Digital PLL Clock Multiplier," Dept of Electroscience, Lund Univerity, Lund, Sweden, date unknown (perhaps 2002), downloaded on 5/24/2004 from http://www.ap-asic.org/2002/proceedings/5B/5B-3.PDF, 4 pages.
	E	T. Olsson and Peter Nilsson, "A Digital PLL made from Standard Cells," Dept of Electroscience, Lund Univerity, Lund, Sweden, date unknown (perhaps 2002), downloaded on 5/24/2004 from http://kontoret.webmaster.se/dockeeperfiles/340/887/A Digital PLL made from Standard Cells.pdf, 4 pages.
	F	D. Abramovitch, "Lyapunov Redesign of Classical Digital Phase-Lock Loops," Agilent Labs, Palo Alto, CA, dated June 5, 2003, downloaded on 5/24/2004 from http://www.labs.agilent.com/personal/Danny Abramovitch/pubs/lpll cdig talk.pdf, 22 pages.

Examiner HAI L. NGUYEN | Date Considered 04/24/2005

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.